IEEE P1581 drastically simplifies connectivity test for memory devices

Heiko Ehrenberg, Chair, IEEE P1581 Working Group
GOEPEL Electronics − Austin, TX / USA
h.ehrenberg@ieee.org

Abstract:

This Poster provides an overview of IEEE P1581, for those not familiar with this standardization effort, and gives a status update of the IEEE P1581 specification development. We will also provide examples for the implementation of IEEE P1581 capabilities in SRAM, DRAM, and FLASH devices.

Introduction

There currently is no defined, independent standard for test technology in memory devices. Each vendor is free to implement test hardware functionality in their ICs (Integrated Circuits) to support **connectivity tests** and built-in self test (**BIST**) any way they choose. Without an independent standard, interoperability amongst ICs is unlikely, jeopardizing reuse of the test technology at board and system levels and, as such, failing to provide the intended test coverage.

IEEE P1581 will provide the specification of protocol and implementation rules for the highest fault coverage and diagnosis of connectivity errors amongst and to/from memory ICs whether in SIPs (System in Package), modules, boards, or systems. It will also provide a specification for test mode access/exit as guidance both to IC vendors implementing IEEE P1581 and to test equipment manufacturers supporting it [1]. IEEE P1581 is aimed at ICs that are otherwise not provisioned with DFT for any reason, targeting primarily memory devices, but also allowing for implementation in other devices.

IEEE P1581 ...
- provides a **simple test logic** implementation for memory devices (and possibly other complex, slave-type components);
- requires **no extra pins**;
- does not rely on complex memory access cycles;
- allows **very fast** test execution with a **small** test vector set; and
- is usable with **any** access methodology (Boundary Scan, functional, ICT).

Motivation

IEEE P1581 is being developed to define a test strategy for memories and other complex devices that do not support IEEE Std 1149.1 in order to verify I/O pin connectivity and enhance testability. Memory devices have been becoming more complex with every generation and this trend will continue. Different kinds of memories present different challenges for test applications above the IC level.

Ideally, connectivity to the memories on a unit under test should be verified - detecting and locating any opens, shorts, and other stuck-at faults before moving on to functional test. Most memory ICs do not implement boundary scan (IEEE Std 1149.1). Therefore, today's conventional approaches utilize a memory's functionality to verify its connectivity - writing a test stimulus pattern into the memory and then reading from the memory to check for the matching response pattern. This creates problems, such as long test execution times, difficulty creating embedded test applications, and reduced quality of diagnostics. In some cases, such an approach may not even be possible. For non-volatile memory devices, for example, a connectivity test based on the devices functionality may result in the erasure of previously programmed data, which would have to be restored after test execution resulting in excessive test execution times.

In an attempt to overcome these problems, the IEEE P1581 working group is defining a protocol and architecture for component interconnection test [2]. While the focus is on memory devices, the same technology can be applied to other slave-type components.

References

[1] Heiko Ehrenberg, *IEEE P1581 Can Solve Your Board-Level Memory Cluster Test Problems*, Proceedings of International Test Conference 2007, Paper 22.3

[2] IEEE P1581 Working Group website http://grouper.ieee.org/groups/1581/